REMARKS/ARGUMENTS

In an Office Action dated September 20, 2007, claims 1-36 were rejected under § 102 over Testardi. Applicants appealed the rejections. On December 11, 2009, the Decision on Appeal affirmed the rejections. Applicants have amended the claims in view of the Decision on Appeal and submit that the amended claims are allowable.

Claim Amendments

Independent claims 1, 19 and 28 have been amended in several areas. First, they have been amended to include a variation of the claim 3 requirement relating to the processors delaying the write operation, with an addition that the delay is performed by the processors holding the write operation and then completing said data write operation without intervention of said control module. Further, they have also been amended to shorten the preamble and to remove the portions related to the coupling to the storage unit.

§ 102 Rejections

Claim 1

As an exemplary claim, Applicants will address the rejection of claim 3 using claim 1 as amended. Claim 1 now includes the requirement that the processors delay a data write operation by holding said data write operation, the operative portion of claim 3 on which Applicants' prior arguments and appeal were based on.

The September 20, 2007 Office Action stated:

> 11.   Regarding claim 3, Edsall and Testardi combined disclose claim 2, and Testardi further discloses wherein table information includes a barrier entry (barrier range) and said processors delay data write operations if said barrier entry relates to said data write operation (retried later, paragraph 207).

The Decision on Appeal stated:

>   4.   Appellants admit that the fast path in Testardi "passes the
> [write] operation on to the control path" (App. Br. 13).
>
>   5.   Testardi teaches that
>
> > [i]f an FP [fast path] is able to dispatch the I/O
> > [input/output] operation further to a particular physical
> > device using a mapping table which is populated by the
> > CP [control path] in this example, the FP does such
> > dispatching without further intervention by the CP.
> > Otherwise, the I/O operation may be forwarded to the CP
> > for processing operations.
>
> (¶ [0074]).

The Decision on Appeal then concluded:

Testardi teaches that when a fast path is unable to dispatch an
input/output (i.e., write) operation, the fast path forwards the operation to the
control path for processing (FF 5). This comports with Appellants'
admission that the fast path in Testardi passes write operations on to the
control path (FF 4).

Appellants argue that these teachings do "not meet the positive
requirements in the claim that the processors perform the delaying
operation" (App. Br. 13). However, claim 3 merely requires that "said
processors delay data write operations" (claim 3; App. Br. 16) and does not
specify the manner of effecting the delay. Moreover, Appellants do not
dispute the Examiner's finding that passing the operation on to the control
path delays the write operations (Ans. 8-9).

For at least these reasons, we find that Appellants have not sustained
the requisite burden on appeal in providing arguments or evidence
persuasive of error in the Examiner's 35 U.S.C. § 102(e) rejection of claim
3, or of claims 12, 17, 18, 21, 26, 27, 30, 35, and 36, which fall therewith,
with respect to this issue.

Applicants specifically note that the Decision indicated that the claim did not meet the arguments being made by Applicants and that the manner of affecting the delay was not specified. Applicants have now amended all of the independent claims to specify the manner of affecting the delay, namely by having the processors hold the data write operation and then complete the data write operation without intervention of the control module.

Testardi indicates that its manner of delay is to send the write operation from the fast path to the control path, where it is later forced to be retried. See ¶ 0207 provided below.

> [0207] Referring now to **FIG. 24**, the CP may then advance the copy barrier range by 1) setting the rmap entry **562** to 1, 2) copying the data from P1 to P2, and 3) setting the rmap entry **566** to 2. Setting a corresponding disk extent indicated by the entry **562** in the table to refer to redirect table entry 2 causes read and write operations to proceed to the second device P2. Any data that has already successfully been migrated to device P2 is accessed through table entry 2. Any data that has not yet begun being migrated to the physical device P2 is accessed through table entry zero with read write operations to P1. Data that is in the process of being migrated within the copy barrier range is accessed through entry 1 with read only operations to device P1. This means that any accesses before or after the copy barrier range, as well as reads to the copy barrier range itself, are satisfied through the FP to P1 or P2. Only a write operation being performed to the copy barrier range itself is actually faulted to the CP to be later retried once the copy barrier range moves to a subsequent extent of the Rmap. The migration is complete when the entire Rmap1 references entry 2 of the redirect table1 at which time entries zero and 1 may be deleted or removed from the redirect table1.

Therefore Testardi operates oppositely from the claim language, where the delay is performed by the processors holding the write operation and then completing said data write operation without intervention of said control module. As such, Testardi does not teach or suggest the current claims.

As the clause "the delay is performed by the processors holding the write operation and then completing said data write operation without intervention of said control module" or similar is in all of the independent claims, including newly added claim 37, all of the independent claims are submitted as being allowable.

CONCLUSION

Based on the above remarks Applicants respectfully submit that all of the present claims are allowable. Reconsideration is respectfully requested.

Respectfully submitted,

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